Model PLL Dynamics And Phase-Noise Performance

By understanding the basic sources of phase noise, it is possible to accurately model a PLL with the help of commercial CAE programs.

Model PLL Dynamics, Part 2

Eric Drucker
PLL Consultants, 7701 56th Ave. NE, Seattle, WA 98115-6301; (206) 525-0674, FAX: (425) 290-1600, e-mail: linerc@sprintmail.com.

PHASE-LOCKED loops (PLLs) and their importance to modern communications were detailed in the first part of this article series (see *Microwaves & RF,* November 1999, p. 69). In that article, a basic PLL model was presented. The loop dynamics were modeled to determine the open- and closed-loop transfer functions and the various loop parameters (such as open-loop gain-crossover, phase margin, closed-loop bandwidth, etc.). An example was presented to illustrate these concepts. In Part 2, the basics of phase noise will be reviewed. Using the mathematical-analysis software MathCAD, along with the previous example, it will be possible to show how the various noise sources in a PLL can be modeled. A novel method using PSPICE to model the noise sources will also be shown.

An amplitude and phase-modulated sinusoidal signal can be written as follows:

$$V(t) = V_0 \cdot [1 + v_{am}(t)] \cdot \{\sin[2\pi f_c t + \theta(t)]\} \quad (6)$$

where:
V_0 = the amplitude,
f_c = the carrier frequency,
$v_{am}(t)$ = the amplitude-modulation (AM) component, and
$\theta(t)$ = the phase-modulation (PM) component.

For the purposes of this discussion, the AM component will be disregarded.

$$V(t) = V_0 \cdot \{\sin[2\pi f_c t + \theta(t)]\} \quad (7)$$

Modeling a sinusoidal-angle modulation with a rate of f_m, yields:

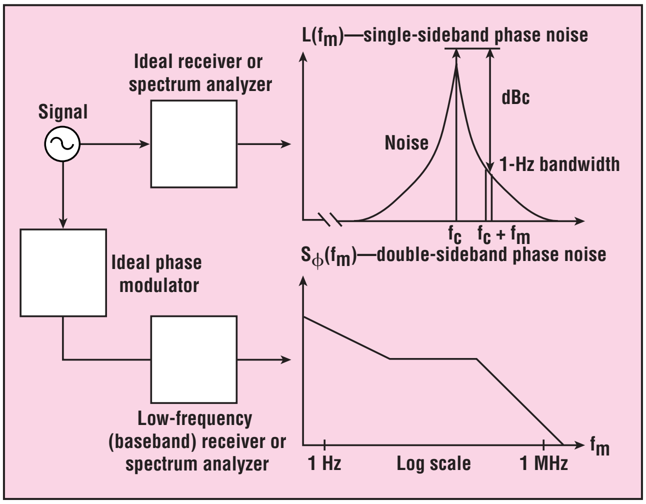
$$\theta(t) = \frac{\Delta f}{f_m} \cdot \sin(2\pi f_m t);\ \beta = \frac{\Delta f}{f_m} \quad (8)$$

$$V(t) = V_o \cdot [\sin(2\pi f_c t) + \beta \sin(2\pi f_m t)] \quad (9)$$

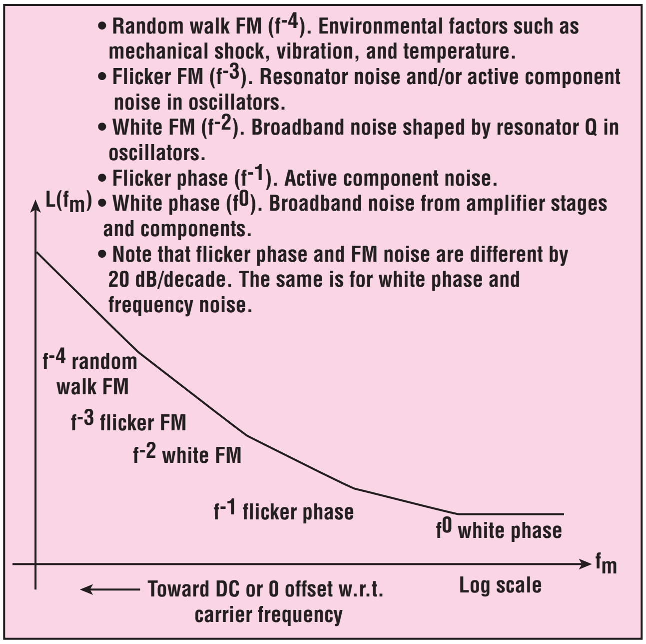
For $\beta \leq 1$ (small-angle modulation) and applying trigonometric identities:

$$V(t) = V_o \cdot [\sin(2\pi f_c t) + \frac{\beta}{2}\{\sin[2\pi(f_c + f_m)] - \sin[2\pi(f_c - f_m)]\}] \quad (10)$$

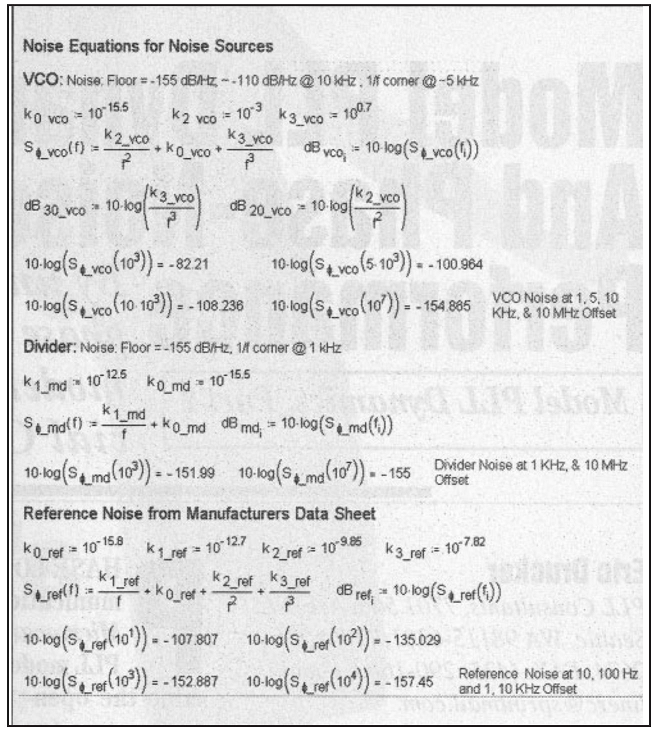
where:
f_m = the modulation frequency,
Δf = the peak frequency-modulation



12. A spectrum analyzer can be used to evaluate single-sideband (SSB) or double-sideband phase noise.



13. Phase noise consists of several components, including random-walk FM, flicker-noise FM, white-noise FM, flicker phase noise, and white phase noise.



Noise Equations for Noise Sources

VCO: Noise: Floor = -155 dB/Hz, ~-110 dB/Hz @ 10 kHz, 1/f corner @ ~5 kHz

$k_{0\_vco} := 10^{-15.5}$ $k_{2\_vco} := 10^{-3}$ $k_{3\_vco} := 10^{0.7}$

$S_{\phi\_vco}(f) := \frac{k_{2\_vco}}{f^2} + k_{0\_vco} + \frac{k_{3\_vco}}{f^3}$ $dB_{vco_i} := 10 \cdot \log(S_{\phi\_vco}(f_i))$

$dB_{30\_vco} := 10 \cdot \log\left(\frac{k_{3\_vco}}{f^3}\right)$ $dB_{20\_vco} := 10 \cdot \log\left(\frac{k_{2\_vco}}{f^2}\right)$

$10 \cdot \log(S_{\phi\_vco}(10^3)) = -82.21$ $10 \cdot \log(S_{\phi\_vco}(5 \cdot 10^3)) = -100.964$

$10 \cdot \log(S_{\phi\_vco}(10 \cdot 10^3)) = -108.236$ $10 \cdot \log(S_{\phi\_vco}(10^7)) = -154.865$ VCO Noise at 1, 5, 10 KHz, & 10 MHz Offset

Divider: Noise: Floor = -155 dB/Hz, 1/f corner @ 1 kHz

$k_{1\_md} := 10^{-12.5}$ $k_{0\_md} := 10^{-15.5}$

$S_{\phi\_md}(f) := \frac{k_{1\_md}}{f} + k_{0\_md}$ $dB_{md_i} := 10 \cdot \log(S_{\phi\_md}(f_i))$

$10 \cdot \log(S_{\phi\_md}(10^3)) = -151.99$ $10 \cdot \log(S_{\phi\_md}(10^7)) = -155$ Divider Noise at 1 KHz, & 10 MHz Offset

Reference Noise from Manufacturers Data Sheet

$k_{0\_ref} := 10^{-15.8}$ $k_{1\_ref} := 10^{-12.7}$ $k_{2\_ref} := 10^{-9.85}$ $k_{3\_ref} := 10^{-7.82}$

$S_{\phi\_ref}(f) := \frac{k_{1\_ref}}{f} + k_{0\_ref} + \frac{k_{2\_ref}}{f^2} + \frac{k_{3\_ref}}{f^3}$ $dB_{ref_i} := 10 \cdot \log(S_{\phi\_ref}(f_i))$

$10 \cdot \log(S_{\phi\_ref}(10^1)) = -107.807$ $10 \cdot \log(S_{\phi\_ref}(10^2)) = -135.029$

$10 \cdot \log(S_{\phi\_ref}(10^3)) = -152.887$ $10 \cdot \log(S_{\phi\_ref}(10^4)) = -157.45$ Reference Noise at 10, 100 Hz and 1, 10 KHz Offset

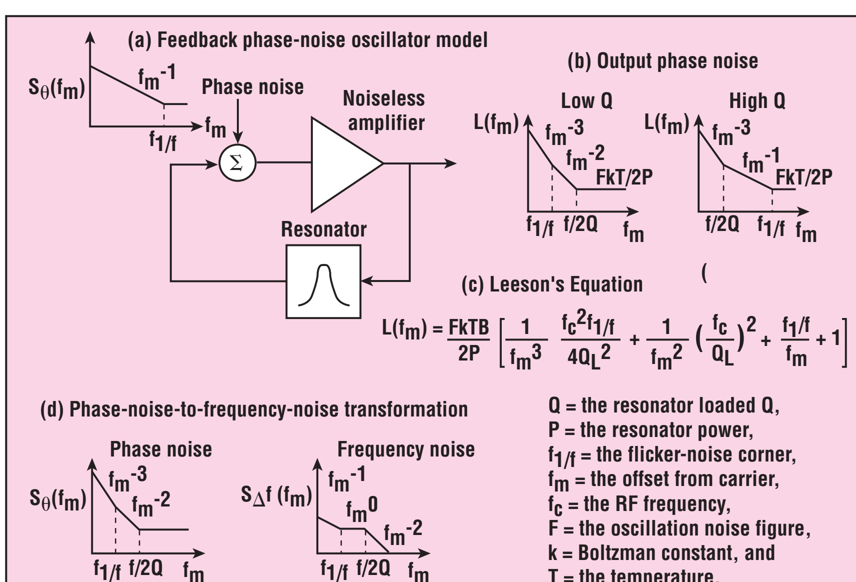
(FM) deviation, and

β = the modulation index.

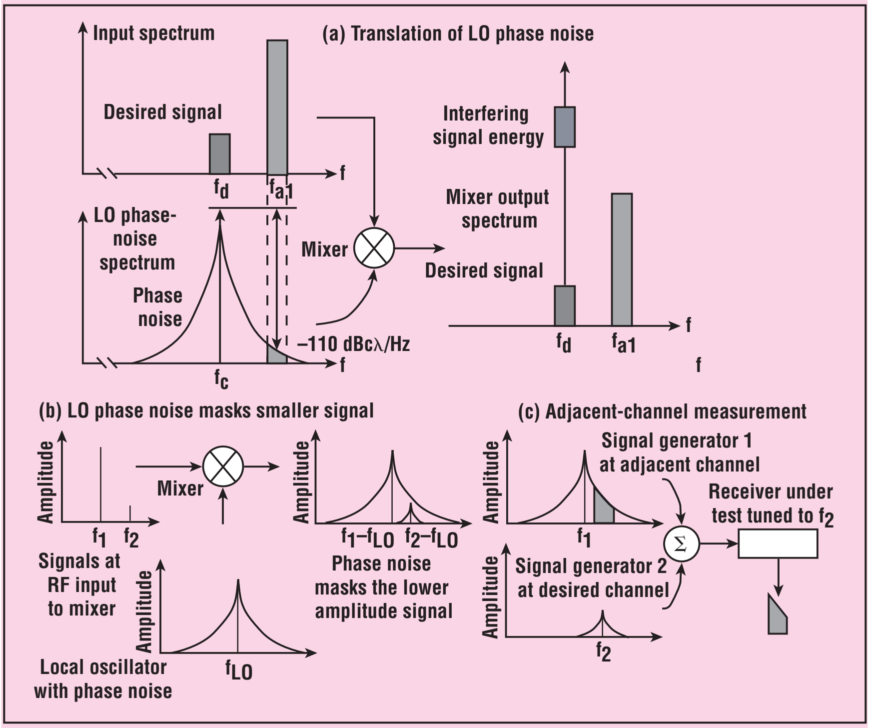
This shows that a small-angle deviation gives rise to sidebands on each side of the carrier at an amplitude of β/2. Extending this idea, noise can be treated as an infinite number of single FM sidebands.

The distribution of these noise sidebands as a function of offset frequency can be expressed in different ways (Fig. 12). One way is to use an ideal receiver or spectrum analyzer at RF with a 1-Hz resolution-bandwidth filter. The total power of the signal would first be measured and, since the noise is small, this is essentially equal to the carrier power. Then the receiver would be tuned to a particular offset (f_m) from the carrier, and the phase-noise power is measured. The ratio of these two measurements, expressed in decibels, is the normalized power-spectral density (PSD) in one sideband referred to the carrier at a frequency offset f_m. This is known as the single-sideband (SSB) phase noise, $L(f_m)$, with units of Hertz^{-1} or expressed in decibels relative to the carrier level as dBc/Hz. A plot of the phase noise as function of the offset is commonly shown in data sheets in order to characterize oscillators and frequency synthesizers.

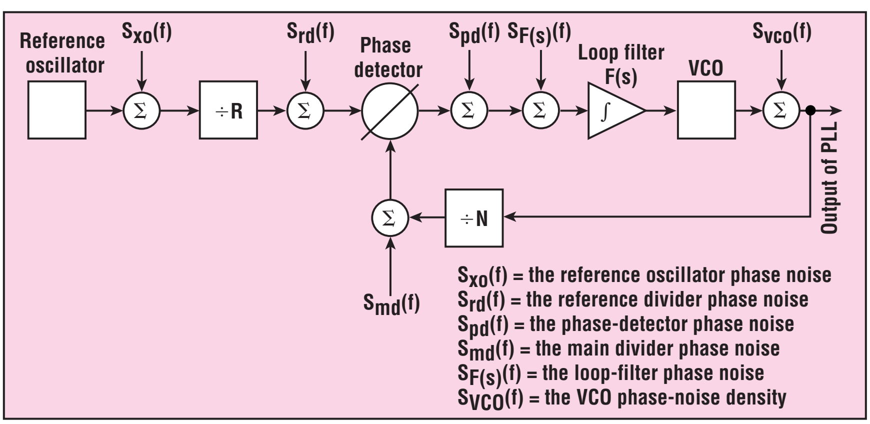
Another method is to demodulate the signal with an ideal phase demodulator. The output of the phase demodulator is the baseband phase noise and can be analyzed with a low-frequency spectrum analyzer, again with a 1-Hz resolution-bandwidth filter. The resulting plot as a function of baseband or offset frequency is the double-sided phase-noise spectrum, $S_\phi(f_m)$, expressed in $(\text{radians})^2$/Hz. The double-sideband phase noise is twice that of (or 3 dB more than) the SSB phase noise. One can integrate the area under the double-sideband phase-noise curve, over a specific bandwidth (f_1 to f_2) to obtain the root-mean-square (RMS) phase noise and, by extension, the RMS frequency noise. From the RMS phase or frequency noise, the



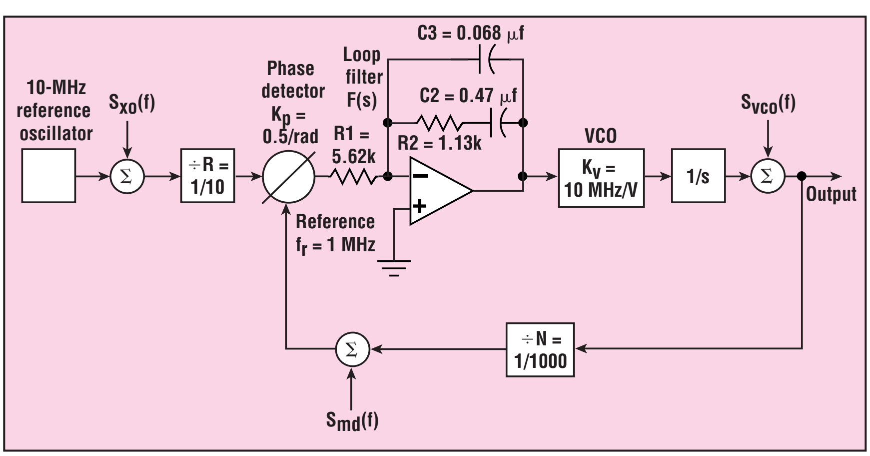
14. An oscillator can be modeled as a feedback system (a) that produces noise as a function of oscillator Q (b). The phase noise can be described in terms of Leeson's equation (c) and transformed to frequency noise (d).



15. An LO's phase noise can affect a receiver's adjacent-channel rejection (a) by masking low-level signals (b). Adjacent-channel performance can be evaluated with a pair of signal generators (c).



16. A variety of noise sources affect the performance of a PLL.



17. In this example, the PLL is assumed to have only three noise sources—VCO noise, reference oscillator noise, and main divider noise.

RMS time jitter can be computed. When looking at phase-noise plots, it should be noted that a "zero" frequency offset or "DC" is the carrier.

The integrated phase noise in terms of RMS radians can be expressed as eq. 11:

$$\Delta\theta_{RMS} = \left[\int_{f_1}^{f_2} S\phi(f_m)df_m\right]^{0.5} \qquad (11)$$

while the integrated frequency noise in terms of RMS Hz can be expressed as eq. 12:

$$\Delta f_{RMS} = \left[\int_{f_1}^{f_2} S\phi(f_m)\cdot f_m^{\,2}df_m\right]^{0.5} \qquad (12)$$

When the phase noise is plotted in decibels versus log frequency, various regions of the phase-noise curve can be identified. These regions have slopes of 0, 1/f (−10 dB/decade), $1/f^2$ (−20 dB/decade), $1/f^3$ (−30 dB/decade), etc. (Fig. 13).

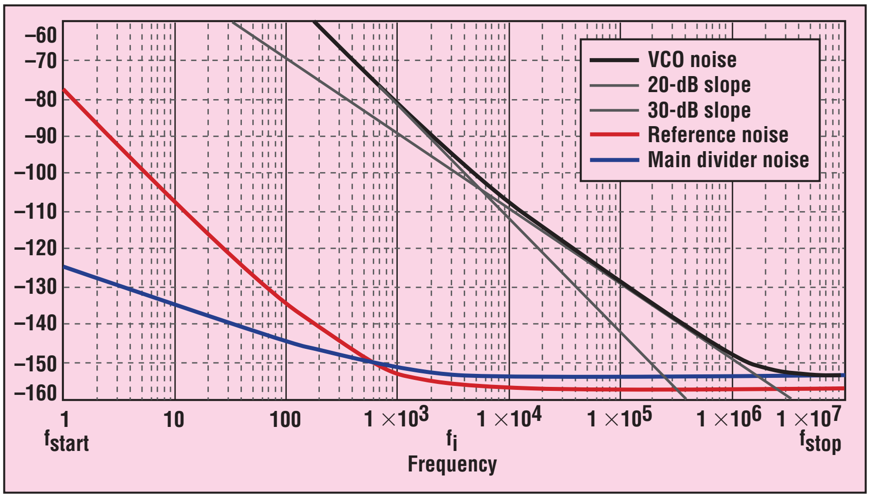
The flat or zero-slope region corresponds to white phase noise of thermal origin. This thermal, resistive, or Johnson noise has a Gaussian amplitude distribution, constant with frequency. Amplifier noise figure is a manifestation of this thermal noise.

Close to "DC" or a zero-frequency offset, there is a region of 1/f, or flicker noise. This is believed to come from irregularities in the semiconductor structure. Typically, the 1/f corner is between 1 and 10 kHz.

Frequency dividers and amplifiers exhibit only 0 and 1/f slope regions. Oscillators can have all regions. The general phase-noise equation shown below (with the m subscript dropped) is typically used for double-sideband noise [$S_\phi(f_m)$] expressed in power:

$$S\phi(f) = k_o + \frac{k_1}{f} + \frac{k_2}{f^2} + \frac{k_3}{f^3} + \frac{k_4}{f^4} \qquad (13)$$

An oscillator can be modeled as a feedback system consisting of a resonator and a noiseless amplifier. Phase noise is injected at the input to the amplifier (Fig. 14a). This injected phase noise consists of a flat region and a 1/f region. This noise is shaped by the resonator, which has a −20-dB/decade



18. This graph shows the phase-noise plots for the three noise sources of the example in Fig. 17.

slope on either side of the center frequency. This flat phase noise becomes $1/f^2$ in nature and the 1/f phase noise becomes $1/f^3$ in nature, within the resonator bandwidth, at the output of the oscillator (Fig. 14b). One could express this noise in terms of frequency or FM noise (Fig. 14d). [It should be noted that the frequency-to-phase transformation is an integration (−20 dB/decade) and, conversely, phase to frequency transformation is differentiation (+20 dB/decade)]. The $1/f^2$ phase noise, (−20 dB/decade), appears as "flat" FM noise and the $1/f^3$ phase noise (−30 dB/decade) appears as flicker FM noise (−10 dB/decade).

Leeson's model (Fig. 14c) describes the phase noise of an oscillator as a function of the resonator-loaded quality factor (Q) or bandwidth, oscillation frequency, noise figure, power, and offset from the carrier. The phase noise improves with higher Q (narrower resonator bandwidth) and power. A lower noise figure and 1/f corner also improves the noise.

Depending on the relative position of the 1/f corner and the resonator bandwidth, two cases arise:

1. In the "low" Q case, typical of most RF/microwave oscillators using inductive-capacitive (LC) tanks, transmission lines, ceramic and dielectric resonators and yttrium-iron garnets (YIGs), the 1/f corner is "inside" (closer to the carrier or "DC") the resonator bandwidth. This gives rise to phase noise plot consisting of three different regions—a flat noise region, a $1/f^2$ region, and then a $1/f^3$ region as shown in Fig. 14b.

2. Crystal oscillators and surface-acoustic-wave (SAW) resonator oscillators have typically very high Qs and, consequently, the phase-noise plot looks slightly different. As before, there is a flat region, but then the 1/f corner is reached first and then the phase noise increases at a rate of 10

Calculate PSPICE Values for Noise Models

$k := 1.38\cdot10^{-23}$ $T := 300$ $q := 1.602\cdot10^{-19}$

$S_{\phi\_vco}(f) := \frac{k_{2\_vco}}{f^2} + k_{0\_vco} + \frac{k_{3\_vco}}{f^3}$ VCO Noise Power Equation

$e_{n0}^2 = 4\cdot k\cdot T\cdot B\cdot R_{k0\_vco}$ $k_{0\_vco} = 4\cdot k\cdot T\cdot B\cdot R_{k0\_vco}$ e_n^2 Represents Noise Power k_{0_vco} Term

$R_{k0\_vco} := \frac{1}{4}\cdot\frac{k_{0\_vco}}{(k\cdot T)}$ Solve for Resistor Values for VCO Flat Noise Component (k_{0_vco})

$R_{k0\_vco} = 1.91\cdot10^4$ $2\cdot R_{k0\_vco} = 3.819\cdot10^4$

$e_{n2}^2 = \left(\frac{K_{i2\_vco}}{f}\right)^2\cdot e_n^2$ Integrating Flat Noise Power to Produce $1/f^2$ Noise Power

$e_{n2}^2 = \frac{\left(K_{i2\_vco}\cdot\sqrt{4\cdot k\cdot T\cdot B\cdot R_{k2\_vco}}\right)^2}{f^2}$ $\left(K_{i2}\cdot\sqrt{4\cdot k\cdot T\cdot B\cdot R_{k2\_vco}}\right)^2 = k_{2\_vco}$ Numerator Equals k_{2_vco}

$K_{i2\_vco} := 10^5$ integrator Gain for VCO $1/f^2$ Noise Component

$R_{k2\_vco} := \frac{1}{4}\cdot\frac{k_{2\_vco}}{(k\cdot T)\cdot K_{i2\_vco}^2}$ Solve for Resistor Values for VCO $1/f^2$ (k_{2_vco}) Noise Component

$R_{k2\_vco} = 6.039\cdot10^6$ $2\cdot R_{k2\_vco} = 1.208\cdot10^7$

$e_{n1}^2 = \left(\frac{k\cdot T}{q\cdot I_D}\right)^2\cdot\frac{K_f\cdot I_D}{f}$ 1/f Noise from PSPICE Diode Noise Model

$K_{i3\_vco} := 10^7$ $I_D := 10^{-3}$ integrator Gain for VCO $1/f^3$ Noise Component & Diode Bias Current

$e_{n3}^2 = \left[\left(\frac{K_{i3\_vco}}{f}\right)^2\cdot\left(\frac{k\cdot T}{q\cdot I_D}\right)^2\cdot\frac{K_f\cdot I_D}{f}\right] = \frac{K_{i3\_vco}^2\cdot\left(\frac{k\cdot T}{q\cdot I_D}\right)^2\cdot\left(K_{f3\_vco}\cdot I_D\right)}{f^3}$

$K_{i3\_vco}^2\cdot\left(\frac{k\cdot T}{q\cdot I_D}\right)^2\cdot\left(K_{f3\_vco}\cdot I_D\right) = k_{3\_vco}$ Numerator Equals k_{3_vco}

Solve for K_f in Diode Model for VCO $1/f^3$ (k_{3_vco}) Noise Component

$K_{f3\_vco} := \frac{k_{3\_vco}}{\left(K_{i3\_vco}^2\cdot k^2\cdot T^2\right)}\cdot q^2\cdot I_D$ $K_{f3\_vco} = 7.505\cdot10^{-14}$

Main Divider

Solve for Resistor Values for Main Divider Flat (k_{0_md}) Noise Component

$R_{k0\_md} := \frac{1}{4}\cdot\frac{k_{0\_md}}{(k\cdot T)}$ $R_{k0\_md} = 1.91\cdot10^4$ $2\cdot R_{k0\_md} = 3.819\cdot10^4$

Solve for K_f in Diode Model for Main Divider 1/f (k_{1_md}) Noise Component

$\left(\frac{k\cdot T}{q\cdot I_D}\right)^2\cdot\left(K_{f1\_md}\cdot I_D\right) = k_{1\_md}$ $K_{f1\_md} := \frac{k_{1\_md}}{\left(k^2\cdot T^2\right)}\cdot q^2\cdot I_D$ $K_{f1\_md} = 4.735\cdot10^{-13}$

Reference

Solve for Resistor Values for Reference Flat (k_{0_ref}) Noise Component

$R_{k0\_ref} := \frac{1}{4}\cdot\frac{k_{0\_ref}}{(k\cdot T)}$ $R_{k0\_ref} = 9.571\cdot10^3$ $2\cdot R_{k0\_ref} = 1.914\cdot10^4$

Solve for K_f in Diode Model for Reference 1/f Noise (k_{1_ref}) Component

$K_{f1\_ref} := \frac{k_{1\_ref}}{\left(k^2\cdot T^2\right)}\cdot q^2\cdot I_D$ $K_{f1\_ref} = 2.988\cdot10^{-13}$

$K_{i2\_ref} := 10^2$ integrator Gain for Reference $1/f^2$ Noise

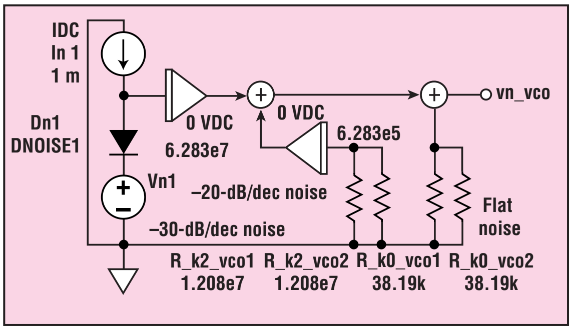
Solve for Resistor Values for Reference $1/f^2$ (k_{2_ref}) Noise Component

$R_{k2\_ref} := \frac{1}{4}\cdot\frac{k_{2\_ref}}{(k\cdot T)\cdot K_{i2\_ref}^2}$ $R_{k2\_ref} = 8.53\cdot10^5$ $2\cdot R_{k2\_ref} = 1.706\cdot10^6$

$K_{i3\_ref} := 10^2$ integrator Gain for Reference $1/f^3$ Noise

Solve for K_f in Diode Model for Reference $1/f^3$ (k_{3_ref}) Noise Component

$K_{f3\_vco} := \frac{k_{3\_vco}}{\left(K_{i3\_vco}^2\cdot k^2\cdot T^2\right)}\cdot q^2\cdot I_D$ $K_{f3\_vco} = 7.505\cdot10^{-14}$



19. The phase noise of a VCO can be modeled using a simple schematic diagram in PSPICE software.

dB/decade. Since the resonator has very high Q, this implies a very narrow bandwidth—less than the flicker corner. Therefore, the region closest to the carrier is the $1/f^3$ region. Even the explanation is somewhat simplified since $1/f^4$ sloped regions have been observed very close to the carrier.

If a PLL is used as a local oscillator (LO) in a receiver, the phase noise of the LO can degrade the adjacent-channel rejection of the receiver by a process known as reciprocal mixing. In Fig. 15a, an input spectrum consisting of the desired signal and a adjacent-channel signal is mixed with an LO. If the LO is only a pure sinusoid, the intermediate-frequency (IF) output of the mixer would just be a shifted replica of the input spectrum. Of course, the IF would have a filter to reject the adjacent channels. The LO phase noise will mix with the unwanted signals in adjacent channels, producing energy that appears in the IF passband, coincident with the desired signal. An example, using the Global System For Mobile Communications (GSM), assumes that the first interfering signal is spaced 600 kHz away and that the detection bandwidth is 200 kHz. If the average LO phase noise is $-110\ dBc/(Hz)^{0.5}$ 600 kHz away, the total noise power in the 200-kHz channel with respect to the carrier is:

$$P = \frac{-110\ dBc/\sqrt{Hz}}{\sqrt{200\ kHz}} = -110 + 10\log(200\ kHz) = -57\ dBc$$

This approximates the noise as being flat across the 200-kHz-wide channel. If the desired signal is −100 dBm and the undesired signal is −60 dBm, the signal-to-noise ratio (SNR) is [−100 dBm − 0 dBc (LO carrier)] − [−60 dBm −57 dBc (LO noise)] = 17 dB. This procedure can be repeated with additional interfering signals to determine the worst-case phase-noise requirement.

In a spectrum analyzer (Fig. 15b), when an attempt is made to resolve two closely spaced signals with widely differing amplitudes, the phase noise of the LO masks the weaker of the two signals. To measure the adjacent-channel selectivity of a receiver, two signal generators are used (Fig. 15c). The amplitude of the in-channel generator is set at the desired sensitivity level and the amplitude of the adjacent or off-channel generator is increased until the sensitivity decreases by a known amount. The phase noise from the adjacent-channel generator that spills into the desired channel could cause the receive selectivity to be worse than expected. The phase noise of the off-channel generator will be measured rather than the in-channel signal. Phase noise can also have an adverse effect in clock-recovery systems, radar, and digital communications systems.

All of the elements in the PLL contribute to the overall phase noise. The noise mechanisms for crystal and RF/microwave oscillators were previously discussed. Another significant source of noise in PLLs is the dividers and phase detectors. There are a number of different types of phase detectors, including mixers or multipliers, sample-and-hold devices, digital exclusive OR gates, and the most common, digital flip-flop phase detectors. The flip-flip phase detector, in addition to providing phase information, also has an intrinsic mechanism to provide proper steering so the loop can achieve lock.

The main disadvantage of the flip-flop phase detector is that it suffers a nonlinear region or "dead zone" close to a zero phase offset. However, various design techniques can mitigate this problem. Other types of phase detectors only provide phase information, and additional circuitry is necessary for steering and acquisition.

LOGIC DEVICES USED FOR PHASE DETECTORS AND DIVIDERS INTRODUCE PHASE NOISE, AND DIFFERENT LOGIC FAMILIES HAVE DIFFERENT PHASE-NOISE CHARACTERISTICS.

The diode mixer phase detector has the best phase noise and is used in critical applications. Logic devices used for phase detectors and dividers introduce phase noise and different logic families have different phase-noise characteristics as a function of the operating frequencies. ECL has a noise floor of approximately −145 to −150 dBc/(Hz)$^{0.5}$, while advanced complementary-metal-oxide-semiconductor (CMOS) logic has a noise floor between −155 and −165 dBc/(Hz)$^{0.5}$ depending on the input (I) and output (O) operating frequency. The 1/f or flicker corner is at an offset frequency of between several hundred Hertz and 10 kHz. In general, faster logic and larger voltage swings give rise to better phase noise. Assuming that the noise is mainly generated in the transition region between logic 0 and 1, with the faster rise time, then less time is spent in the transition region, resulting in lower noise levels.

Since advanced CMOS logic has a +5-VDC swing versus approximately 800 mV for ECL, this would explain the noise improvement when using advanced CMOS logic. It is difficult to measure the phase noise of dividers and

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phase detectors due to the low noise levels involved. Some manufacturers of single-chip PLLs provide noise-floor results.

Other sources of noise in the PLL include operational amplifiers (opamps) used for loop filters and noise from power supplies. These noise sources are shown in Fig. 16. The loop operates on these various noise sources. It is possible to write the Laplace transfer function, substituting s = j2πf from each of these noise sources to the output. The magnitude of the transfer function squared multiplied by the phase-noise equation of the source, expressed in power, provides the output phase-noise power of that source at the output of the loop. By superposition, it is possible to power sum the effects of all the individual noise sources in order to produce a composite output phase-noise curve.

NOISE CAN BE MODELED USING PSPICE ELEMENTS, BUT IT IS NECESSARY TO TRANSFORM THE NOISE EQUATION FOR THE VARIOUS NOISE SOURCES IN THE PLL.

MODELING NOISE

Using the previous example (Fig. 17), assume that the PLL has only three noise sources—voltage-controlled-oscillator (VCO) noise, reference-oscillator noise, and main-divider noise. It is desirable to express these noise sources in terms of double-sideband phase-noise power [(radians²/Hz]. The VCO has a noise floor of −155 dB/Hz, a 1/f corner frequency of 5 kHz, and a specified noise of approximately −110 dB/Hz at an offset frequency of 10 kHz. The coefficients of the phase-noise equation (equation 13) were manually adjusted in the MathCAD program to yield the specified phase noise at the particular offsets from the carrier. These are shown in the accompanying sidebar (see "Noise Equations for Noise Sources") on page 74 with some representative values for the noise at particular offsets.

The main divider has a floor of −155 dBc/_Hz and a 1/f or flicker corner of 1 kHz. The 10-MHz reference noise was obtained from the data sheet for a commercial 10-MHz temperature-compensated crystal oscillator (TCXO). The four coefficients in the reference-noise equation were experimentally determined using asymptotic lines with 0, −10-, −20-, and −30-dB/decade slopes in MathCAD to best approximate the noise plot from the manufacturer's data sheet. The phase-noise plots, in decibels, of these three sources are displayed in Fig. 18.

In Part 1, PSPICE was used to model the loop dynamics of a PLL. Noise can also be modeled by using PSPICE elements. First, it is necessary to transform the noise equation for the various noise sources in the PLL (VCO noise, reference noise, etc.), into PSPICE elements. Resistors produce "flat" noise and the diode model in PSPICE has a term for 1/f or flicker noise (−10 dB/decade). By integrating the flat resistor noise, it is possible to produce $1/f^2$ (−20 dB/decade) noise and by integrating the diode noise (1/f), it is possible to produce $1/f^3$ (−30-dB/decade) noise. Each term in the noise equation can be represented by one of the PSPICE elements mentioned, or a combination of elements. This concept will be illustrated by modeling the VCO noise in the example (Fig. 19).

Next month, the third and final installment of this article series on modeling PLL dynamics and noise will show how to combine the different noise sources to review what has been learned and to show how to integrate the knowledge of phase-noise contributors to produce a final phase-noise curve for the example loop.●●