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Model PLL Dynamics And Phase-Noise Performance

Model PLL Dynamics, Part 1

A popular mathematical modeling tool and SPICE software can simplify the analysis of phase-locked loops.

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PHASE-LOCKED loops (PLLs) have become a mainstay in modern electronics. Until recently, due to their high cost, their use has been confined to military and high-end commercial hardware and high-performance RF test equipment. With the advent of the "wireless revolution" of the last decade, however, PLLs are now widely used in consumer applications, notably cellular telephones and communications systems where good phase noise is critical. This first installment of a three-part article series will review the fundamentals of PLLs. The calculation of loop dynamics, which affects noise performance, will also be covered. In the next installment, the basics of phase-noise concepts will be reviewed.

Before it is possible to predict the phase noise of a PLL, it is necessary to understand the dynamics of the PLL system. A PLL is basically a control system, where phase is the variable of interest. It can be analyzed using classical linear Laplace transform techniques. Recall that the Laplace transform is a shorthand method for representing a linear differential equation with constant coefficients, with variable s representing the differentiation operator. This linear model is really all that is needed to analyze the noise, modulation, and small-signal switching performance of a PLL (Fig. 1).

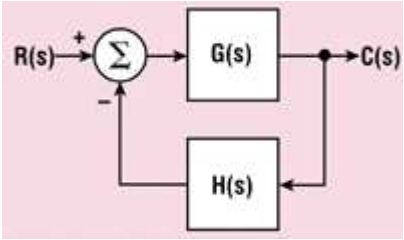


Fig 1. This simple control system can be used to emulate the operation of a PLL.

In its simplest form the system consists of a forward-gain block G(s) and a feedback block H(s). The open-loop gain is G(s)H(s) and the system transfer function or closed-loop gain is:

$$C(s)/R(s) = (Forward\_Gain)/(1 + Loop\_Gain) = G(s)/[1 + G(s)H(s)] \quad (1)$$

By using this simple rule, it is possible to easily write transfer functions for loops with multiple forward and feedback blocks to obtain the transfer function from virtually any input to output. Using signal-graph theory, one can also analyze loops within loops, although this is not necessary for most PLL applications.

By taking the inverse Laplace transform, the small-signal time-domain performance can be predicted, such as the PLL's small-signal frequency and phase-settling time as well as the final phase error. It is possible to apply a step (1/s) or other forcing function at the input, R(s), to see how the system behaves. Even without taking the inverse Laplace transform, only using the transfer function by itself, the initial and final value theorem gives insight into limits of time-domain performance at t = 0 and t = when excited by step, ramp, etc.

To view the response of the system in the frequency domain, or the small-signal sinusoidal steady state, the Laplace transform variable s need only be replaced by j to produce Bode plots. These Bode plots lend considerable insight into the performance of a control system. One can analyze the open-loop gain and phase response and be able to predict the performance and stability of the loop when it is closed, which will ultimately determine the noise performance. The stability is important as it affects the amount of peaking in the closed-loop response and in the extreme can lead to loop oscillations. The poles are in the denominator of the transfer function, while the zeros are in the numerator. Each pole yields a -6-dB/octave or -20-dB/decade slope on a Bode plot. A zero results in a similar positive slope.

Only the poles in the denominator of the closed-loop transfer function impact stability. The denominator of the closed-loop transfer function is 1+ G(s)H(s) or 1 + open-loop gain. If the magnitude of the open-loop gain approaches unity at the same time the phase approaches 180 deg., this indicates a potential for instability, as the denominator of the transfer function will tend toward zero. The denominator of the closed-loop transfer function is not affected by where the stimulus is applied in the loop and which output is being observed. Taking these control-theory concepts and applying them to a PLL yields the linearized control system model for a PLL, consisting of a phase detector, loop-filter voltage-controlled oscillator (VCO), and divider (Fig. 2).

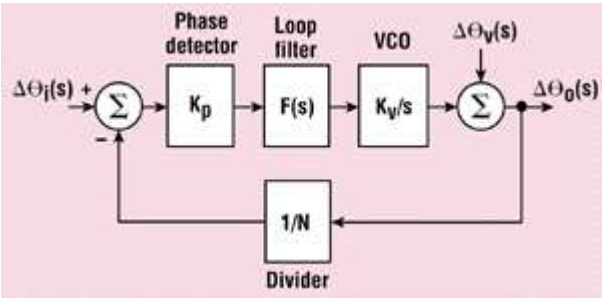


Fig 2. A simple PLL model can be constructed with a phase detector, loop filter, VCO, and divider.

Referring to Fig. 2, the forward gain, G(s), is equal to KpF(s)(Kv/s). The feedback gain, H(s), is equal to 1/N. The loop gain, G(s)H(s), is equal to:

$$G(s)H(s) = K_p F(s)(K_v / s) / (1 / N) \quad (2)$$

Therefore, the closed-loop transfer function with respect to the input phase is:

$$\frac{\Delta\theta_o(s)}{\Delta\theta_i(s)} = K_p F(s)\frac{K_v}{s} \Big/ 1 + K_p F(s)\frac{K_v}{s}\frac{1}{N} = N\left[\frac{K_p F(s)K_v}{N} \Big/ s + \frac{K_p F(s)K_v}{N}\right] \quad (3)$$

The closed-loop transfer function with respect to phase perturbations introduced at the VCO's output is:

$$\frac{\Delta\theta_o(s)}{\Delta\theta_v(s)} = 1 \Big/ 1 + K_p F(s)\left(\frac{K_v}{s}\right)\left(\frac{1}{N}\right) = s \Big/ s + \frac{K_p F(s)K_v}{N} \quad (4)$$

It should be noted that this is a baseband model of a PLL. The carrier, or RF frequency, does not enter into the analysis. What this transfer function represents what happens to the phase of the output signal from the VCO if one "wiggles," or modulates, the phase of the reference signal into the phase detector. This lowpass transfer function also predicts how the loop acts on noise from the reference, phase detector, and divider. Note that at "DC" that gain is N. The second transfer function represents what happens to the phase of the output of the loop if a phase perturbation at the VCO output is introduced. The 1 in the numerator is the forward-path gain. This highpass transfer function predicts how the loop will act on VCO noise.

The VCO has a transfer function of Kv/s. In other words, a VCO acts as a "pure" integrator in a PLL. This comes about because a VCO is a voltage-to-frequency converter. The VCO tuning coefficient (Kv) is typically expressed in MHz/V. To convert the frequency output of the VCO to the phase variable, one applies the relationship that d/dt = . In other words, phase is the integral of frequency with respect to time. This accounts for the 1/s, the ideal integrator, in the VCO's transfer function.

Taking this frequency to phase relationship one step further, it is possible to redraw the block diagram is terms of frequency deviation. The 1/s ideal integration of the VCO is moved to the feedback block, G(s), and the input frequency is transformed to phase by the addition of an ideal integrator before the phase detector (Fig. 3).

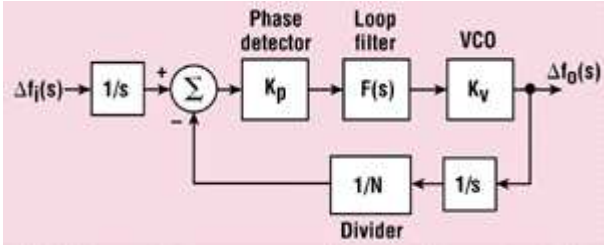


Fig 3. This alternative model for a PLL rearranges the ideal integrator (1/s) in its transfer function.

By applying the control-system rule, the transfer function is:

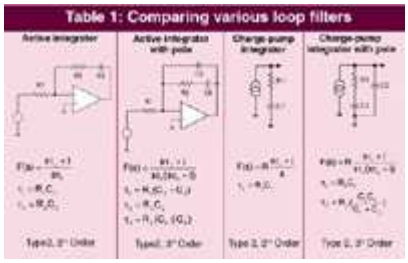
$$\frac{\Delta f_o(s)}{\Delta f_i(s)} = \frac{1}{s}(K_p F(s) K_v) / 1 + (K_p F(s) K_v)\frac{1}{s}\frac{1}{N} = N\left[\frac{\frac{K_p F(s) K_v}{N} / s +}{\frac{K_p F(s) K_v}{N}}\right] \quad (5)$$

This transfer function is the same as before. The only difference is the placement of the 1/s integration blocks. In other words, frequency modulating the reference frequency and observing the frequency deviation at the VCO has the same transfer function as phase modulating the reference frequency and observing the phase deviation at the VCO.

In both models, the phase detector is broken up into two blocks--an ideal subtractor and a phase to voltage converter. There are many types of phase detectors (mixer, multiplier, sample and hold, digital exclusive OR, and digital phase/frequency), but the most common is a digital phase/frequency detector. The phase-detector range is approximately ±2 with a gain of Kp = Vp/2 for a voltage output configuration and Kp = Ip/2 for a current output configuration. This type of phase detector has the advantage in that it acts similar to a frequency steering device when the loop is not locked. It can "tune" the VCO close enough to the frequency required for locking. Pure phase detectors, such as a mixer, require additional circuitry in the PLL to steer to VCO close to the correct frequency. The divider in the feedback path has a gain of 1/N.

The loop filter or F(s) block ultimately determines the dynamics of the PLL. In the simplest PLL, the phase detector is connected directly to the VCO, where F(s) = 1, but almost all PLLs use some form of an active integrator as a loop filter. An integrator allows the correct VCO voltage with almost zero phase error at the phase detector, which minimizes the reference energy and hence lowers the reference spurious. The integration response (-20 dB/decade) does not extend indefinitely out in frequency. There is a break, or zero, in the transfer function caused by the addition of an R in series with the integrator capacitor. This break is necessary for loop stability. The form is different depending on whether the phase detector has a voltage or current output.

The operational amplifier (opamp) circuitry is for use with a voltage-output phase detector. Most commercial single-chip PLL synthesizers have a charge pump, or current output. The equivalent loop-filter block does not need an active element to perform the integration. Some of the various types of loop filters are shown in Table 1.



The F(s) block can be made quite elaborate by the addition of active or inductor-capacitor (LC) filtering following the integrator. These blocks are useful for filtering of noise or spurious signals. PLLs are often specified in terms of the type and order. The type indicates the number of integrators or poles at DC. It should be pointed out that the virtual pole due to the VCO's frequency-to-phase integration counts for 1. The order is the total number of poles. The simplest PLL without a F(s) block is a Type I, first-order loop.

Including an additional integrator in the F(s) block yields a Type II, second-order loop. Placing an additional pole with the integrator in the F(s) block gives a Type II, third-order loop. These are the most-common loops.

SETTING AN EXAMPLE

Some of these basic PLL concepts and some additional new ideas can be demonstrated with an example. The example of Fig. 4 consists of a voltage-output phase detector with a reference frequency of 1 MHz, an active integrator, a VCO with Kv of 10 MHz/V, and a feedback division ratio of 1000.

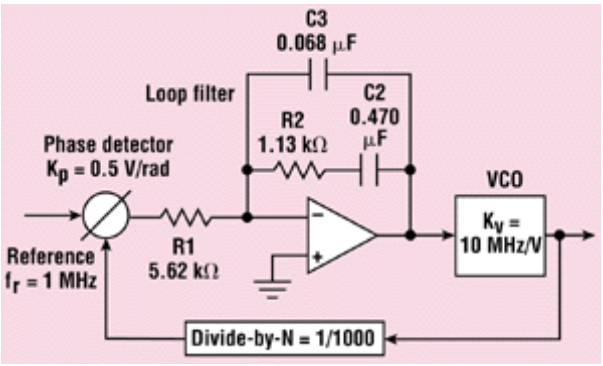


Fig 4. For the purpose of analysis, this example PLL was used. It consists of a voltage-output phase detector, an active integrator, a VCO, and divider.

Therefore, the output frequency is 1 GHz. Usually, it is desired to change the output frequency, so that N is not constant but, in this case, a nominal value of 1000 is assumed.

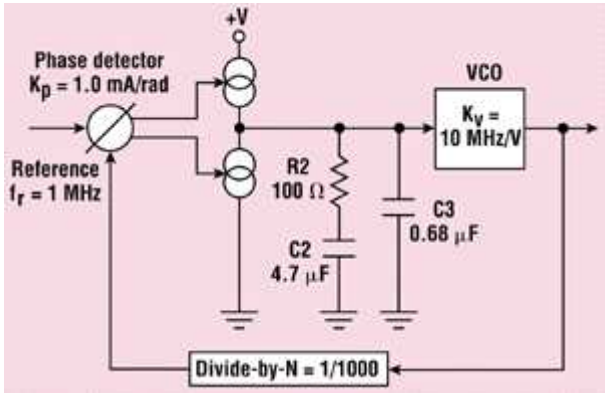
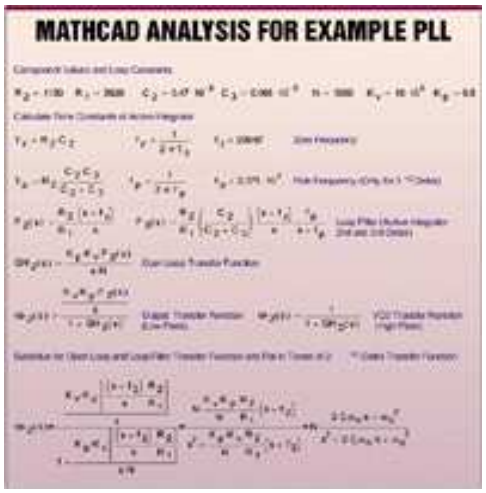


Fig 5. The PLL can also be modeled with a current-output phase detector.

An equivalent version using a current-output phase detector is shown in Fig. 5, although the voltage source version will serve as an example.



The derivation of the loop equations using MathCAD are shown in the sidebar.

The time constants are first calculated for the active integrator. Two cases are presented--a second-order case (where C3 is set to 0) and a third-order case. The open-loop and closed-loop transfer functions are shown in terms of the Laplace variable s. The loop filter can be expressed in terms of time constants, as shown in Table 1, or pole/zero frequencies, as shown in the sidebar.

The gain-crossover frequency is the frequency at the point the magnitude of the open-loop gain equals 1 or 0 dB [|GH(j)} = 1]. The first-order gain crossover frequency is a useful quantity. This is the gain as if this were a first-order loop with the same loop parameters (Kv, Kp, and N), but F(s) is equal to the gain of the loop filter.

This is arrived at by setting the open loop zero(s) = 0 (DC) and the open-loop pole(s) = . The gain crossover is equal to approximately 1 kHz for this example.

For the second-order case, it is possible to express the closed-loop transfer function in terms of the natural frequency (n) and damping factor (xi). This is a holdover from classical control theory. It should be stressed that this approach is not very useful for higher-order loops.

Creating Bode plots with MathCAD is very straightforward. A log frequency sweep is generated and s is set to j. Since MathCAD performs all the algebraic and complex number housekeeping, most of drudgery is eliminated.

Figure 6 shows the filter response and the PLL open-loop gain for the second- and third-order cases.

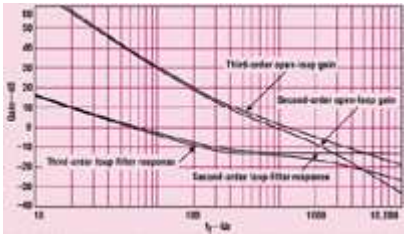


Fig 6. The loop-filter and open-loop gain responses are plotted for the second- and third-order cases of the example.

The filter response shows the 20-dB/decade slope from the active integrator, flattening out at the zero frequency of 300 Hz. For the third-order case, the response once again drops at 20-dB/decade starting at the pole frequency of 2.3 kHz. The PLL open-loop gain is "tilted" by 20-dB/decade due to the virtual integration in the loop from the VCO. The slope before the zero is 40-dB/decade, changing to 20-dB/decade. For the third-order case, it changes back to 40-dB/decade after the pole. The response crosses unity gain (0 dB) with a slope of approximately 20-dB/decade.

The phase response is shown in Fig. 7.

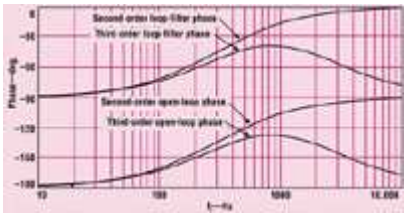


Fig 7. The loop filter and open-loop phase responses are plotted for the second- and third-order example cases.

For the filter, the phase shift that is close to DC is -90 deg. After the zero, the phase approaches 0 deg. and, for the third-order case, climbs back up to -90 deg. after the pole. The PLL's open-loop phase differs from the filter by -90 deg. and starts at -180 deg. and approaches -90 deg. for the second-order case. It then goes back to -180 deg. for the third-order case.

The phase margin is probably the best indication of loop stability. It is defined as the phase shift, with respect to -180 deg. at the gain crossover frequency. Using the root-finding function in MathCAD, it is possible to set the magnitude of the open-loop transfer function equal to unity, [|GH(j)| = 1], then allow MathCAD to find the frequency. The computed values are summarized in Table 2.

Table 2: Computer loop parameters

	Second-order case	Third-order case
Gain crossover frequency	1345 Hz	872 Hz
Phase margin	74 deg	31 deg
Lowpass closed-loop -3-dB frequency	1292 Hz	1450 Hz
Highpass closed-loop -3-dB frequency	752 Hz	926 Hz

The phase margin is computed from this gain crossover by determining the argument of the open-loop phase and subtracting it from 180 deg. A true first-order loop will provide 90 deg. of phase margin.

The addition of the zero and pole decreases the phase margin from 90 deg. The closer the pole or zero is to the gain-crossover frequency, the worse that the phase margin becomes. The zero is typically placed at approximately one-third of the gain-crossover frequency and a pole should be placed greater than two times the gain-crossover frequency. Usually, it is best to have at least 45 deg. of phase margin in order to minimize the peaking in the frequency domain and overshoot in the time domain.

Figure 8 shows the closed-loop response.

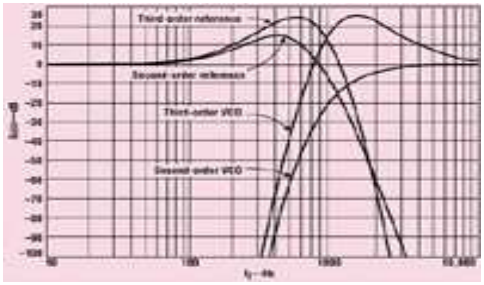


Fig 8. The closed-loop gain is plotted for the reference and VCO second- and third-order cases.

For the lowpass case, the DC gain of M is normalized to 1. The third-order case shows more peaking in the highpass and lowpass responses consistent with the reduced phase margin. Once again, MathCAD can be used in order to calculate the 3-dB frequencies by setting the magnitude of the appropriate closed-loop transfer function that is equal to 0.701 (-3 dB).

Using circuit-simulation programs, such as PSPICE, similar results can be obtained as those calculated with MathCAD. As a check, it is useful to model the PLL both ways to see if the results are consistent. The PSPICE model is shown in Fig. 9.

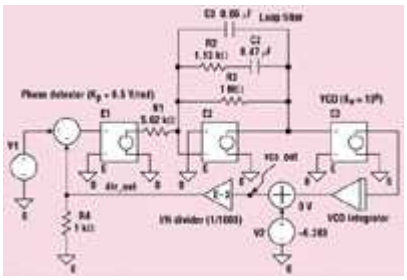


Fig 9. This PSPICE schematic diagram includes the VCO integrator, phase detector, and loop filter.

The PLL elements, phase detector, loop filter, VCO, and divider are modeled as voltage-controlled voltage sources (VCVS). The phase detector is broken up into a subtractor and a Kp gain block. The opamp is idealized using a high-gain (105) VCVS.

The 1 M resistor in the model of Fig. 9 enables PSPICE to converge when measuring the open-loop gain. The VCO is another VCVS with a gain of Kv. The virtual VCO integrator provides a gain of -2 to convert Kv from Hertz to radians. A sign change is included in this block to guarantee negative feedback. In a real PLL, one would interchange the variable as well as reference inputs to the phase detector to obtain the proper phase. Finally, the divider is a gain block with a gain of 1/N.

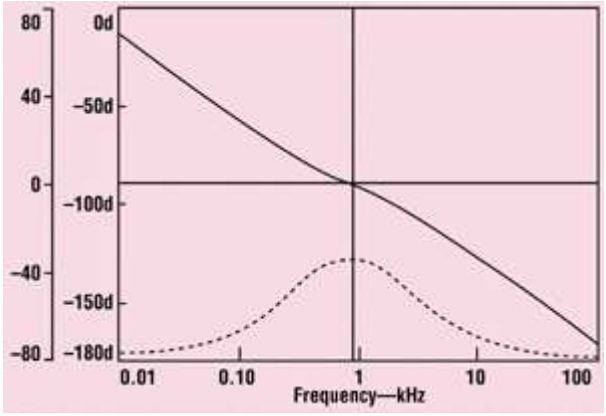


Fig 10. The PSPICE circuit simulator was used in order to predict the open-loop gain and phase responses of the example PLL.

To measure the open-loop gain and phase, the loop would be broken at R4 and the stimulus applied at V1 and measured at div_out. To measure the lowpass closed-loop gain, the stimulus is applied at V1 and measured at vco_out. The highpass response is obtained by stimulating at V2 and measuring at vco_out (Figs. 10 and 11).

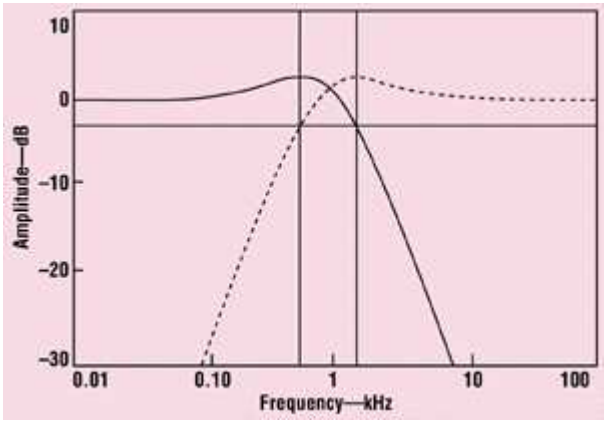


Fig 11. The PSPICE circuit simulator was used to predict the closed-loop response of the example PLL.

The next installment in this article series on PLLs will review the sources of phase noise, and extend the concepts of loop modeling to predicting the phase-noise performance of the loop. MathCAD and a SPICE simulator will be used in the modeling process